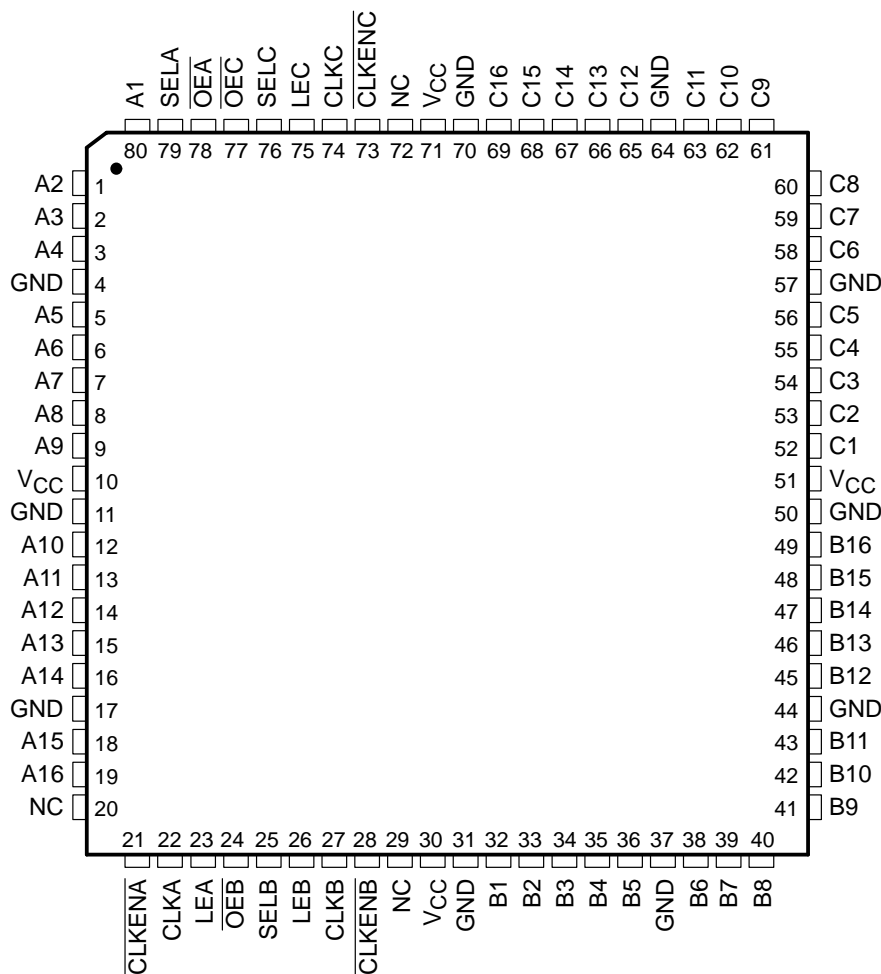


# SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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- Members of the Texas Instruments *Widebus+*™ Family
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- *UBE*™ (Universal Bus Exchanger) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 80-Pin Plastic Thin Quad Flat (PN) Package With  $12 \times 12\text{-mm}$  Body Using 0.5-mm Lead Pitch and 84-Pin Ceramic Quad Flat (HT) Package

'ABTH32316 . . . PN PACKAGE  
(TOP VIEW)



NC – No internal connection



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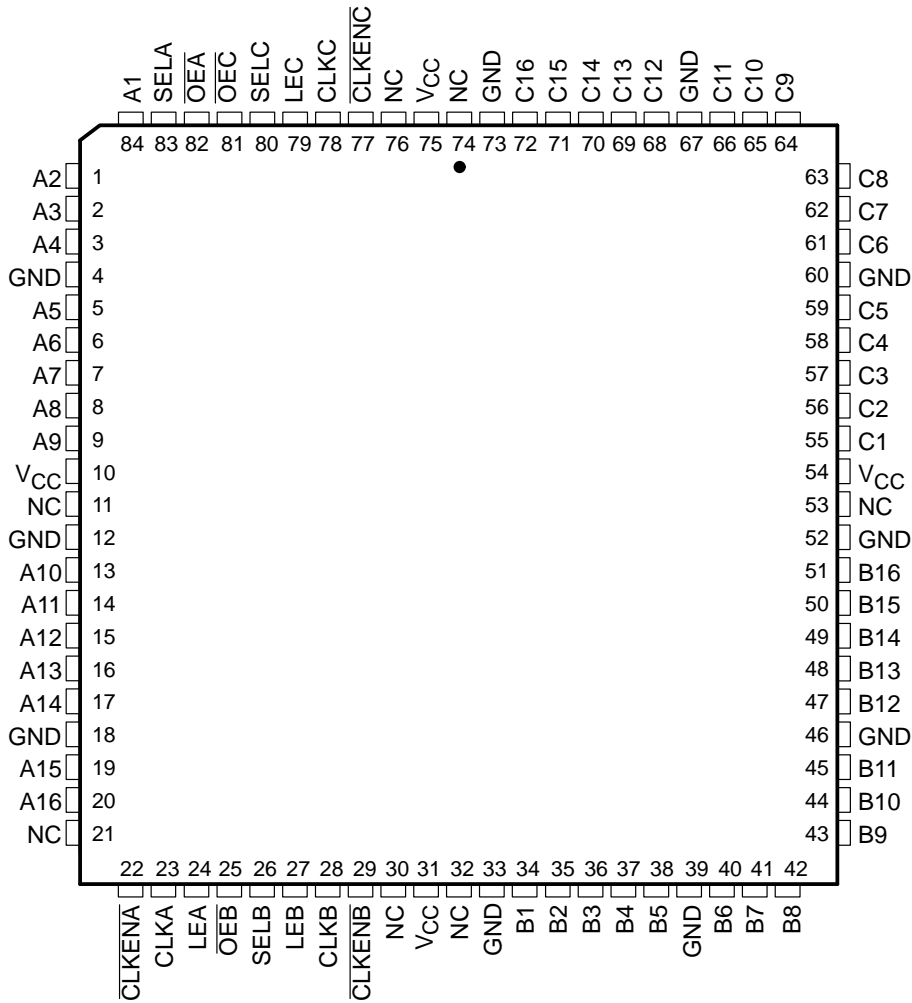
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# SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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SN54ABTH32316 . . . HT PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The 'ABTH32316 consist of three 16-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable ( $\overline{OEA}$ ,  $\overline{OEB}$ , and  $\overline{OEC}$ ), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA and clock-enable A ( $\overline{CLKENA}$ ) are low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



# SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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## description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH32316 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  
The SN74ABTH32316 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### Function Tables

#### STORAGE†

INPUTS				OUTPUT
$\overline{\text{CLKENA}}$	CLKA	LEA	A	
H	X	L	X	$Q_0^{\ddagger}$
L	$\uparrow$	L	L	L
L	$\uparrow$	L	H	H
X	H	L	X	$Q_0^{\ddagger}$
X	L	L	X	$Q_0^{\ddagger}$
X	X	H	L	L
X	X	H	H	H

† A-port register shown. B and C ports are similar but use  $\overline{\text{CLKENB}}$ ,  $\overline{\text{CLKENC}}$ ,  $\text{CLKB}$ ,  $\text{CLKC}$ ,  $\text{LEB}$ , and  $\text{LEC}$ .

‡ Output level before the indicated steady-state input conditions were established

#### A-PORT OUTPUT

INPUTS		OUTPUT A
$\overline{\text{OEA}}$	SELA	
H	X	Z
L	H	Output of C register
L	L	Output of B register

#### B-PORT OUTPUT

INPUTS		OUTPUT B
$\overline{\text{OEB}}$	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

#### C-PORT OUTPUT

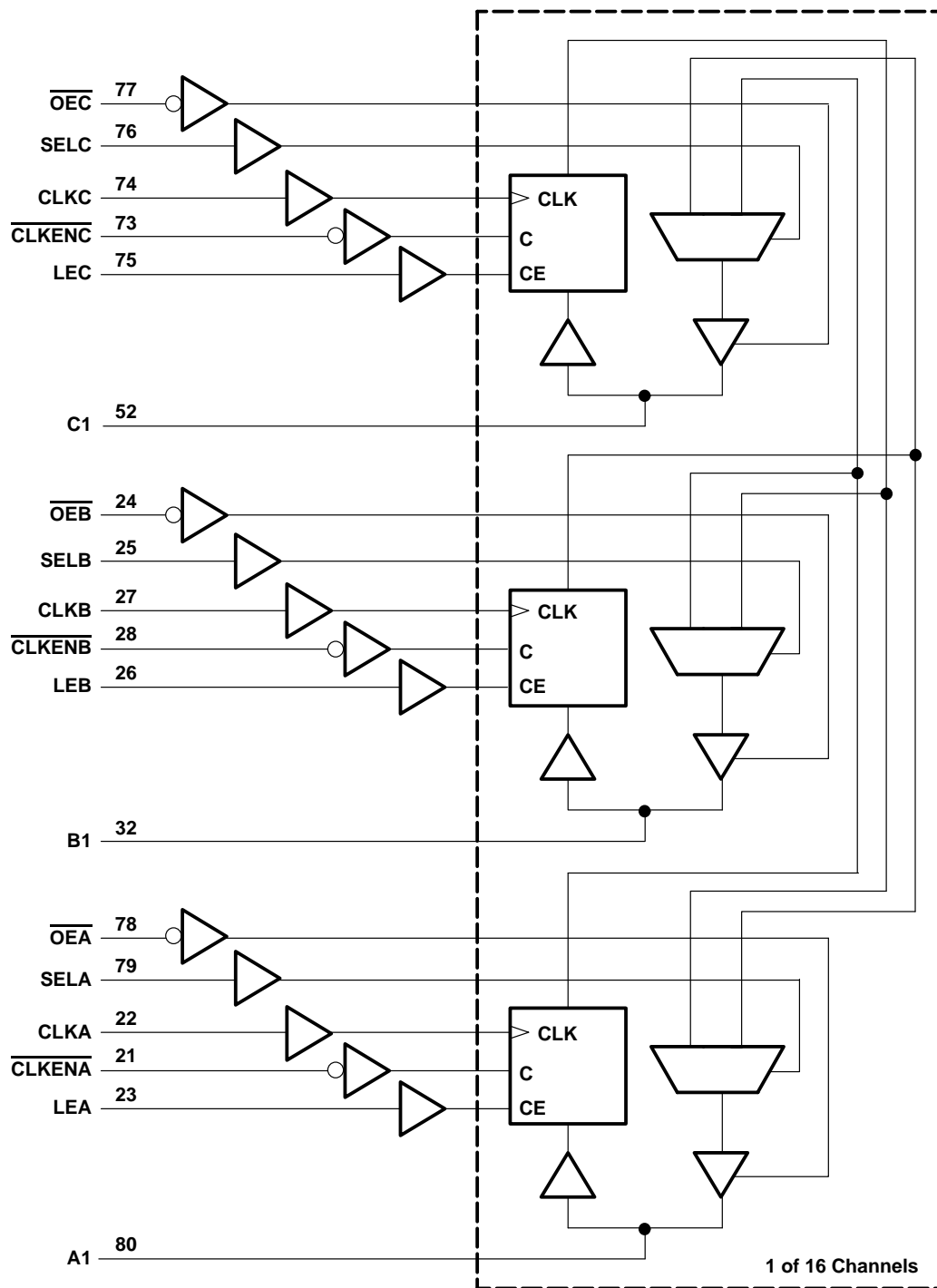
INPUTS		OUTPUT C
$\overline{\text{OEC}}$	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register



# SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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## logic diagram (positive logic)



Pin numbers shown are for the PN package.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABTH32316 .....	96 mA
SN74ABTH32316 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): PN package .....	62°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABTH32316		SN74ABTH32316		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



# SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH32316			SN74ABTH32316			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$			2.5			2.5	V
		$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$			3			3	
		$V_{CC} = 4.5\text{ V}$			2			2	
$V_{OL}$		$V_{CC} = 4.5\text{ V}$			0.55				V
								0.55	
$V_{hys}$					100			100	mV
$I_I$	Control inputs	$V_{CC} = 0\text{ to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$			$\pm 1$	$\mu\text{A}$
	A, B, or C ports	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 100$			$\pm 20$	
$I_I(\text{hold})$	A, B, or C ports	$V_{CC} = 4.5\text{ V}$			100			100	$\mu\text{A}$
					-100			-100	
$I_{OZPU}^\ddagger$		$V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$			$\pm 50$	$\mu\text{A}$
$I_{OZPD}^\ddagger$		$V_{CC} = 2.1\text{ V to }0$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$			$\pm 50$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or }V_O \leq 4.5\text{ V}$			$\pm 100$			$\pm 100$	$\mu\text{A}$
$I_{CEX}$		$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$			50			50	$\mu\text{A}$
$I_O^\S$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-100	-180	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$			2			2	mA
				40			40		
				1			1		
$\Delta I_{CC}^\parallel$		$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1			0.5	mA
$C_i$	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$			3			3	pF
$C_{io}$	A, B, or C ports	$V_O = 2.5\text{ V or }0.5\text{ V}$			11.5			11.5	pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This parameter is specified by characterization.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABTH32316		SN74ABTH32316		UNIT
			MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency		0	150	0	150	MHz
$t_w$	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
$t_{su}$	Setup time	A, B, or C before $\text{CLK}\uparrow$	2.6		2.4		ns
		A or B before $\text{LE}\downarrow$	2.5		2.1		
		CLKEN before $\text{CLK}\uparrow$	3.5		3.2		
$t_h$	Hold time	A, B, or C after $\text{CLK}\uparrow$	1.8		1.4		ns
		A or B after $\text{LE}\downarrow$	2.4		2.1		
		CLKEN after $\text{CLK}\uparrow$	1.5		1.1		



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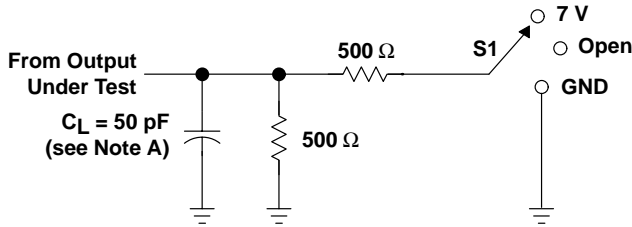
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABTH32316		SN74ABTH32316		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			150		150		MHz
$t_{PLH}$	A, B, or C	C, B, or A	0.8	6.5	1.4	6.1	ns
$t_{PHL}$			0.5	6.8	1.1	6.6	
$t_{PLH}$	SEL	A, B, or C	0.8	6.7	1.4	6.5	ns
$t_{PHL}$			0.8	6.8	1.8	6.5	
$t_{PLH}$	LE	A, B, or C	1.5	8	2.6	7.5	ns
$t_{PHL}$			1.5	7.4	2.6	6.9	
$t_{PLH}$	CLK	A, B, or C	1.5	8	2.5	7.5	ns
$t_{PHL}$			1.5	7.2	2.5	6.7	
$t_{PZH}$	$\overline{OE}$	A, B, or C	0.8	6.7	1.5	6.4	ns
$t_{PZL}$			1.5	7.1	2.4	6.8	
$t_{PHZ}$	$\overline{OE}$	A, B, or C	0.8	7.2	1.5	6	ns
$t_{PLZ}$			0.8	6.4	1.9	6.1	

# SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

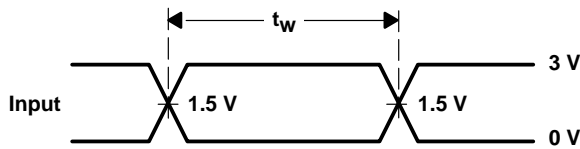
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## PARAMETER MEASUREMENT INFORMATION

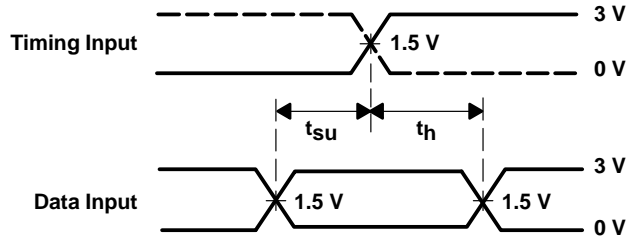


LOAD CIRCUIT

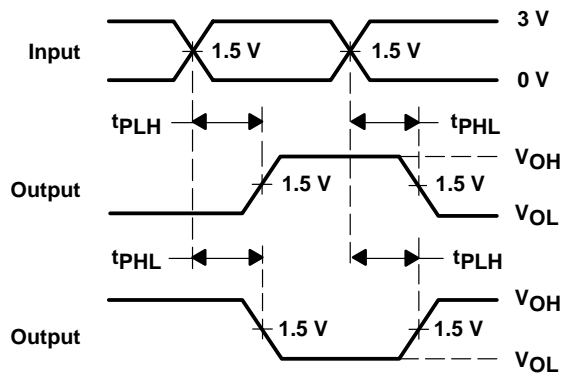
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



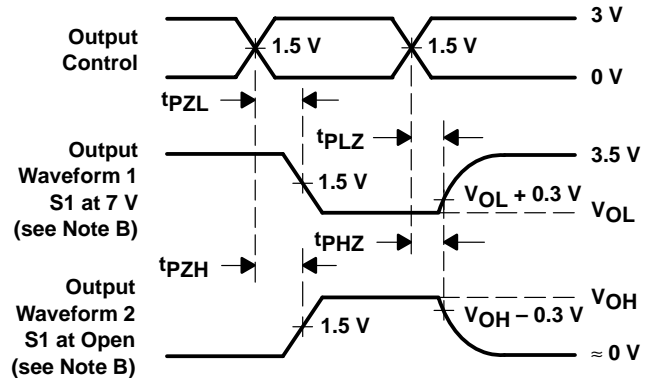
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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